Claims 1-2, 4-5, 7-9, 15, 17, 19, 20, and 40-41 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Merrill et al. (US 6,512,544) in view of Sauer (US 6,320,616). This rejection is respectfully traversed. In order to establish a *prima facie* case of obviousness "the prior art reference (or references when combined) must teach or suggest all the claim limitations." M.P.E.P. §2142. Neither Merrill et al. nor Sauer, even when considered in combination, teaches or suggests all limitations of independent claims 1 and 15.

Claim 1 recites a method of processing pixel signals comprising, *inter alia*, "clamping a pixel readout line to a voltage level less than a voltage corresponding to a pixel signal; subsequently coupling the pixel readout line to an output of a source-follower transistor and reading out the pixel signal onto the pixel readout line; [and] subsequently clamping a capacitive storage node in a pixel signal processing circuit to a voltage less than a voltage corresponding to the pixel signal appearing on the pixel readout line" (emphasis added). Claim 15 recites similar limitations for an imager. Applicants respectfully submit that the Merrill et al. and Sauer combination does not teach or suggest these limitations.

To the contrary, Sauer teaches that the highest possible value of the Col_Read(x) line is 3.801V, and the voltage is lowered by the pixel signal readout. Col. 8, ln. 18-19. Activation of clamp line CL, "causes the APS reference voltage of 3.801 V to be applied to node 157." Col. 7, ln. 38-39 (emphasis added). "The voltage (3.801 V) on the Col_Read(x) line at this stage may be referred to as the APS reference voltage, since it serves as a reference to measure the voltage difference which will be caused when the photo signal charge is transferred to FD node 115." Col. 7, ln. 17-21. Therefore, the first step in Sauer is setting the column output line to a high voltage level.

Although the Office Action refers to Merrill et al. to teach the limitation of "clamping a pixel readout line to a voltage level less than a voltage corresponding to a pixel signal" and "subsequently coupling the pixel readout line to an output of a source-follower transistor and reading out the pixel signal onto the pixel readout line," using the other steps in Sauer would destroy the functionality of both Merrill et al. and Sauer. Thus, the reference are not combinable to read on the claimed invention. Since the circuit of Merrill et al. is designed to read a rising pixel signal, it cannot read the falling pixel signal of Sauer.

Moreover, although the Office Action claims in the Response to Arguments section that Sauer teaches "clamping the capacitive storage node (157) to a voltage less than a voltage correspond[ing] to the pixel signal appearing on the pixel readout line," Sauer actually teaches that "the voltage at node 157 **falls** by 1 V, which change is indicative of the amount of light sensed." Col. 8, ln. 23-24 (emphasis added). This indicates that node 157 necessarily started at a voltage higher than the pixel level. Therefore, Applicants respectfully submit that Sauer does not disclose, teach, or suggest "clamping a capacitive storage node ... to a voltage less than a voltage corresponding to the pixel signal appearing on the pixel readout line," as recited in claims 1 and 15. The Office Action admits that Merrill et al. fails to teach or suggest these limitations. Thus, Merrill et al. does not remedy the deficiencies of Sauer.

The Office Action further asserts that the clamping of the storage node occurs after the pixel signal is coupled to the readout line. However, the only time the clamp signal is activated is when node 157 is set to a high voltage of 3.801 V. Col. 7, ln. 38-39. Pixel readout occurs later. Col. 8, ln. 13-16.

Furthermore, it should be noted that Sauer FIG. 1 shows that the Col_Read(x) column line is always connected to the output of the source follower transistor M3, so the pixel readout line is coupled to the output of the source follower before the clamping can occur.

The Supreme Court held in *KSR Int'l Co. v. Teleflex Inc.* that "the [Graham] factors continue to define the inquiry that controls" a finding of obviousness and reiterated that a "patent composed of several elements is not proved obvious merely by demonstrating that each element was, independently, known in the prior art." 127 S.Ct. 1727, 1734 (U.S. 2007). The Graham factors include determining the scope and content of the prior art, ascertaining differences between the prior art and the claims at issue, and resolving the level of ordinary skill in the pertinent art. *Graham v. John Deere*, 383 U.S. 1, 148 USPQ 459 (1966).

Since Merrill et al. and Sauer, even when combined, do not teach or suggest all of the limitations of claims 1 and 15, claims 1 and 15 are not obvious over the cited references. Claims 2, 4-5, 7-9, 17, 19, 20, and 40-41 depend, respectively, from independent claims 1 and 15, and are patentable at least for the reasons mentioned above, and on their own merits. Applicants respectfully request that the 35 U.S.C. § 103(a) rejection of claims 1-2, 4-5, 7-9, 15, 17, 19, 20, and 40-41 be withdrawn and the claims allowed.

In view of the above, Applicants believe the pending application is in condition for allowance.

Dated: October 21, 2008

Respectfully submitted,

By #44198

Thomas J. D'Amico
Registration No.: 28,371
Rachael Lea Leventhal
Registration No.: 54,266
DICKSTEIN SHAPIRO LLP
1825 Eye Street, NW
Washington, DC 20006-5403
(202) 420-2200
Attorneys for Applicants